

CLAIMS:

1. A phase locked loop arrangement comprising an oscillator circuit (240) controlled in response by a signal of a phase or frequency detection circuit (210), said phase locked loop circuit further comprising:
 - a) first timer means (110) for receiving a predetermined threshold frequency;
 - 5 b) second timer means (112) for receiving an output frequency of said oscillator circuit (240);
 - c) change control means (130) for generating a blocking signal in response to the outputs of said first and second timer means (110, 112), and
 - d) blocking means (260) for suppressing supply of said output signal towards
 - 10 said oscillator circuit (240) in response to said blocking signal.
2. An arrangement according to claim 1, further comprising reference oscillator means (20) for generating said threshold frequency.
- 15 3. An arrangement according to claim 1 or 2, wherein each of said first and second timer means comprise a counter circuit (110, 112), and wherein said threshold frequency and said output frequency are supplied to respective clock inputs of said counter circuits (110, 112).
- 20 4. An arrangement according to any one of the preceding claims, wherein said change control means comprise a finite state machine (130) for receiving respective carry signals of said first and second timer means (110, 112), the finite state machine being configured to generate said blocking signal and a reset signal for resetting said first and second timer means (110, 112) in response to at least one of said carry signals.
- 25 5. An arrangement according to claim 4, wherein said finite state machine (130) comprises a logic circuit (136) adapted to generate a logic signal from which said blocking signal is derived, an wherein said logic signal is active when both carry signals are active, or

when said reset signal and said blocking signal are active, or when said reset signal is not active and said blocking signal is active.

6. An arrangement according to claim 4 or 5, wherein said finite state machine (130) has a first state (NBC) during which said first and second timer means (110, 112) are operated and said blocking signal is not active, a second state (NBR) during which said reset signal is active to reset said first and second timer means (110, 112) and said blocking signal is not active, a third state (BC) during which said first and second timer means (110, 112) are operated and said blocking signal is active, and a fourth state (BR) during which said reset signal is active to reset said first and second timer means (110, 112) and said blocking signal is active.

7. An arrangement according to any one of claims 4 to 6, wherein said blocking signal and said reset signal are latched by respective flip-flop circuits (132, 134), to which said output frequency is supplied as a clock signal.

8. An arrangement according to any one of the preceding claims, wherein said blocking means comprises controllable switching means (260) for switching a connection between said detection circuit (210) and said oscillator circuit (240).

9. An arrangement according to any one of the preceding claims, wherein said threshold frequency is an upper threshold frequency and said output signal is used to increase said output frequency of said oscillator circuit (240).

10. An arrangement according to any one of claims 1 to 8, wherein said threshold frequency is a lower threshold frequency and said output signal is used to decrease said output frequency of said oscillator circuit (240).